PERSONAL INFORMATION

ZAYER Fakhreddine

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Sex Male | Date of birth 05/10/1989 | Nationality Tunisian

PERSONAL STATEMENT

PhD in Electrical and Electronics Engineering

Research Master's Degree in Materials, Nanostructures, Devices and microelectronic systems

EDUCATION AND TRAINING

Oct 2021: PhD degree at University of Monastir, Tunisia with Prof. Hamdi Belgacem, in collaboration with Prof. Antonio Maffucci; for the PhD's project " Emerging memory technologies: Modeling and Applications "

Jan2019–April2019: Research Mobility Scholarchip funded by Erasmus + Internationnal Credit Mobility Program within Prof. Antonio Maffucci's Group, Department of Electrical and Information Engineering, University of Cassino and Southern Lazio, Cassino, Italy (http://www.eng.unicas.it/)

Main activities (supervised by Prof. Antonio Maffucci):

- Reliability Analysis and Variation-Aware Simulator for Memory crossbar designs.

May2018–Jul 2018: 3rd PhD internship at the Institute of telecommunication of Aveiro, University of Aveiro, Aveiro, Portugal (https

Main activities (supervised by Prof. José Carlos Pedro):

- Linearization techniques and analog predistorters for Power Amplifier using memristors.

May 2017–Jul 2017: 2nd PhD internship at the Institute of telecommunication of Aveiro, University of Aveiro, Aveiro, Portugal (https://www.it.pt/)

Main activities (supervised by Prof. José Carlos Pedro):

- Linearization techniques and analog predistorters for Power Amplifier using memristors.

Apr 2015–June 2015: 1st PhD internship at Institute of Microelectronics, University of Sevilla, Sevilla, Spain (CNM-IMSE http://www.imse-cnm.csic.es/)

Main activities (Supervised by Prof. Bernabe Linares Barranco and Prof. Teresa Serrano-Gotarredona):

- Neuro-inspired demonstration with bipolar memristive switching devices and their associated circuit design systems in cadence platform**.**

2014/2015: Research contract at Integration of Materials to the System (IMS) Lab, University of Bordeaux, Bordeaux France (http://www.ims-bordeaux.fr/) within Cristel Maneux's group (nanoelectronics); Team(Model): compact modeling and characterization of electronic devices (https://www.ims-bordeaux.fr/fr/recherche/groupes-recherche/29-nanoelectronique/12-nanoelectronique)

Main activities (supervised by Prof. Cristel maneux):

- Compact modelling of memristive devices (i.e. ReRAM, PCM, FTRAM, CBRAM…),
- Optimization techniques and extraction device parameters using the IC-CAP software (Integrated Circuit Characterization and Analysis Program).

2013: Diploma of research Master's Degree: Materials, Nanostructures, Devices and microelectronic systems. Microelectronics and Instrumentations Lab, at the Faculty of Science of Monastir, Monastir –Tunisia, with Distinction (16 /20). Final average of Master's degree: 12.51/20. Number of acquired credits: 106 /120.

Master's Thesis Project: Contribution to the modeling of memristor devices and potential applications

- Comprehension of physics and electrical modelling (Spice, Matlab & Simulink) of redox based TiO2 memristors
- Memristor based Chaotic Oscillators
- Memristor based digital application

June 2011: Diploma of basic Bachelor's degree in physics
Faculty of Sciences of Monastir, Monastir (Tunisia)

June 2008: Baccalaureate Degree
High School of Ouled Chemekh, Mahdia (Tunisia)
Section: Experiemental Sciences

PROFISSIONNAL & WORK EXPERIENCE

RESEARCH EXPERIENCE

Research Projects

Since 2021: Post-doctoral researcher in Hardware for AI at Khalifa university, KUCARS Center.

The objective of the research focus is to propose, implement constrained resource device & architecture for smart AI robotics. This includes IoT Algorithms, Security for Robotics, as well as autonomous robotics

❖ **April 2019: Research Associate in Electronic Engineering at Khalifa University: ADEK Award for Research Excellence. Project about RRAM - Based Computational Intelligence Hardware for IoT.**

- The objective is to investigate the suitability of memristor to perform machine and deep learning for pattern recognition and computer vision applications
- Innovative use of the memristive crossbar to compute local intensity changes (i.e. compute and store brightness differences between neighboring pixels, i.e. spatial gradients).
- Designs for accumulation of data through a pseudo-parallel in-memory computing architecture.
- Low power and efficient on-chip solution of the image enhancement algorithm.

❖ **2016: Compact modeling of Resistive switching for RRAMs and neuromorphic applications (PhD)**

- Modelling of oxide-based resistive switching for non-volatile memory applications and neuromorphic circuits.
- Use of electronic circuits for an increased understanding of the human brain and the development of electronic systems for e-Health, with focus on mental health. Development of neuromorphic circuits and systems mimicking the behavior and learning processes in animals and humans.

❖ **2017: Reliability Analysis and Variation-Aware Simulator for Memory crossbar designs(PhD)**

- Impact of reliability phenomena of the memory crossbar designs. This quantification will through more light to memory designer to design more robust memory crossbar designs.
- 3-D electrothermal modeling for signal and thermal integrity analysis of 3-D stacked Resistive-switching random access memory (RRAM) arrays.
- New biasing schemes or new materials and alternative materials, such as carbon nanotube and copper to deals with voltage drops along interconnects and thermal crosstalks in 3D monolithic RRAM based integrated design.

❖ **2018: Viability of using Nonlinear Memristive System in Analog Neural Network Predistorsion Linearizer Design for Future 5G Wireless Transmitters(PhD)**

- The design and the implementation of a series of a Volterra series as a reconfigurable memristive crossbar neural network that combines the computation and memory together and breaks through the 'memory wall' bottleneck to adaptively predistort the input I/Q base-band waveforms at low computational cost with low energy consumption for future 5G telecommunications networks.

Participation in R&D projects at Khalifa university

- **2020: Abu Dhabi Award for Research Excellence. Project about Efficient Accelerators for 3D Point Cloud Deep Learning for Real-Time Underwater Scene Analysis Applications**
  - ✓ Design and implementation of efficient hardware accelerators for 3D point cloud deep learning for real-time underwater scene analysis applications
- Research on point cloud data on different deep learning algorithm recently used for real-time object segmentation and classification that need to rely on accurate, efficient real-time and robust perception of the underwater environment and pick up the suitable ones for the targeted hardware accelerators.
- Develop hardware architecture for the selected DL on 3D point cloud algorithms with different cross-layer network topologies. This will include :
- In-memory computing using traditional and/or emerging memories and compute elements.
- Approximate computing techniques such as the reduced precision computation, on loop perforation, and relaxed synchronization.
- Assess the performance of the hardware accelerators based on the following objectives:
- End-to-end performance: Parallel computation, high utilization, high data bandwidth
- 3D based DL model accuracy: As accurate as high-precision implementations
- Power efficiency: Application power should be dominated by compute elements

❖ **2020: CIRA project about an Alternative Numbering Systems and Fused Arithmetic for Deep Learning Hardware Implementation**

- Alternative number systems such as LNS and RNS will be utilized to build optimized architectures for the core operations of DNNs such as multiply add accumulate and dot-product operations, the inherent ease of performing multiplication operations in LNS and RNS will be exploited to realize small and efficient DNN architectures.
- The concept of fused-arithmetic will be extended to alternative numbering systems to further enhance efficiency and achieve similar or better accuracy when compared to traditional numbering systems.
- A set of novel deep learning AI algorithms suited for edge devices will be identified. The chosen algorithms will be optimized to suit hardware implementation in the alternative representations. These algorithms will be implemented in traditional numbering systems and alternative numbering systems for proper comparison.
- Dedicated single chip accelerators using alternative numbering systems and fused arithmetic will be developed emphasizing tensor products and direct sum operations, for increased accuracy and reduction of complexity of DNN implementation. These accelerators can be used stand alone or easily integrated with other products in the form of soft or hard IPs.

❖ **2019: CIRA project about a Scalable Haptic based-neuromorphic vision system enabling Near- and In-memory computing for AI hardware**

- Convolutional Spiking Neural Networks (CSNN) as a neuromorphic accelerator to process and train the event-driven classifier that should be capable of yielding good classification results when using real data captured from DVS chips.
- Mapping of the DVS input output with the CSNN processor and analyze system performance such as total event activity and network latencies, which are relevant for eventual hardware implementations.

Pipelining and implementation of the event-based processing in FPGA that allows uncorrelated-event noise removal and real-time tracking of multiple objects, with dynamic capabilities to adapt itself to fast or slow and large or small objects.

Peer-reviewed Journal Publications

[1] Fakhreddine Zayer, Khitem Lahbacha, Alexander Melnikov, Hamdi Belgacem, Massimiliano de Magistris, Wael Dghais, and Antonio Maffucci' Signal and Thermal Integrity Analysis of 3D Stacked Resistive Random Access Memories, accepted in IEEE Tran on Elec. Devices, 23 Oct 2020. **(Q1)**

[2] F. Zayer, B. Mohammad, H. Saleh, and G. Gianini, "RRAM Crossbar-Based In-Memory Computation of Anisotropic Filters for Image Preprocessing," *IEEE Access*, vol. 8, pp. 127569–127580, 2020, doi: 10.1109/ACCESS.2020.3004184. **(Q1)**

[3] Z. Fakhreddine, W. Dghais, and H. Belgacem, "Modeling framework and comparison of memristive devices and associated STDP learning windows for neuromorphic applications," *J. Phys. Appl. Phys.*, 2019, doi: 10.1088/1361-6463/ab24a7. **(Q1)**

[4] F. Zayer, W. Dghais, M. Benabdeladhim, and B. Hamdi, "Low power, ultrafast synaptic plasticity in 1R-ferroelectric tunnel memristive structure for spiking neural networks," *AEU - Int. J. Electron. Commun.*, vol. 100, pp. 56–65, Feb. 2019, doi: 10.1016/j.aeue.2019.01.003. **(Q1)**

[5] W. Dghais, M. Souilem, F. Zayer, and A. Chaari, "Power Supply- and Temperature-Aware I/O Buffer Model for Signal-Power Integrity Simulation," *Mathematical Problems in Engineering*, Aug. 08, 2018. https://www.hindawi.com/journals/mpe/2018/1356538/. **(Q2)**

[6] Benabdeladhim M, Zayer F, Dghais W, Hamdi B. An Efficient Fault Tolerance Technique for Through-Silicon-Vias In 3-D Ics. International Journal of Advanced Computer Science and Applications. 2018 Jul 1;9(7):264-70. **(Q2)**

[7] F. Zayer, H. Abdelneba, B. Mohammad, and G. Gianini,'' **Memristor based IMC architecture for Random Spray Retinex Hardware implementation**. under revision J. IEEE on image processing **(Q1)**.

[8] Zayer, H. Salim, and B. Mohammad,'' **Memristor based IMC architecture of Camur interpolation based image zooming application.**Under preparation. under revision J. IEEE Signal processing letter **(Q1)**

[9]. F. Zayer, H.F. Amira, B. Mohammad, H. Saleh and G. Gianini,'' Memristor based IMC state machine for edge-aware filtering based image preprocessing; FPGA implementation. IEEE TCAS Journal **(Q1**).

[10] Zayer F, Dghais W and Hamdi B, "Physics-based Compact Modeling for Metal-Insulator-Metal Memristive Devices", under revision J. Phys. Appl. Phys journal **(Q1)**

Peer-reviewed Conference

[1] F. Zayer, W. Dghais, and H. Belgacem, "TiO2 memristor model-based chaotic oscillator," in 2017 24th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Dec. 2017, pp. 54–57, doi: 10.1109/ICECS.2017.8292024

[2] K. Lahbacha, F. Zayer, W. Dghais, A. Maffucci, and H. Belgacem, "Reliable 3D 1D1R-1R1D Solution for Victim Layers in Monolithic RRAM Integration," in 2020 IEEE International Conference on Design Test of Integrated Micro Nano-Systems (DTS), Jun. 2020, pp. 1–4, doi: 10.1109/DTS48731.2020.9196043

[3] F. Zayer et al., "Thermal and Signal Integrity Analysis of Novel 3D Crossbar Resistive Random Access Memories," in 2019 IEEE 23rd Workshop on Signal and Power Integrity (SPI), Jun. 2019, pp. 1–4, doi: 10.1109/SaPIW.2019.8781680.

[4] F. Zayer et al., "Electrothermal Analysis of 3D Memristive 1D-1RRAM Crossbar with Carbon Nanotube Electrodes," in 2019 IEEE International Conference on Design Test of Integrated Micro Nano-Systems (DTS), Apr. 2019, pp. 1–6, doi: 10.1109/DTSS.2019.8915266.

[5] F. Zayer, W. Dghais, and H. Belgacem, "Improved TiO2 TEAM Model Using a New Window Function," in 2018 30th International Conference on Microelectronics (ICM), Dec. 2018, pp. 236–239, doi: 10.1109/ICM.2018.8704104..

[6] K. Lahbacha, H. Belgacem, W. Dghais, F. Zayer, and A. Maffucci, "Electrothermal RRAM Crossbar Improvement with 3-D CRS and 1D1R-1R1D Architectures," in 2021 IEEE International Conference on Design Test of Integrated Micro Nano-Systems (DTS), Jun. 2021, pp. 1–5. doi: 10.1109/DTS52014.2021.9498259.

[7] K. Lahbacha, H. Belgacem, W. Dghais, F. Zayer, and A. Maffucci, "High Density RRAM Arrays With Improved Thermal and Signal Integrity," in 2021 IEEE 25th Workshop on Signal and Power Integrity (SPI), May 2021, pp. 1–4. doi: 10.1109/SPI52361.2021.9505230.

Book Chapter

[1] F. Zayer, W. Dghais, and H. Belagcem, "Modeling of Memristive Devices for Neuromorphic Application," in Real-Time Modelling and Processing for Communication Systems: Applications and Practices, M. Alam, W. Dghais, and Y. Chen, Eds. Cham: Springer International Publishing, 2018, pp. 175–202.

RESEARCH SUPERVISION

- **Co supervisor of a PhD student Meriem Bettayeb at Khalifa university, uae,** for the research project: In-memory computing architectures for computer vision application
- **Co supervisor of a PhD student Khitem Lahbacha at the university of southern Lazio, Italy** for the research project 3D memory crossbar design-Reliability and Analysis.

- **Co supervisor of a Master student at Imec institute- Netherland** for the research project Sparce coding-for efficient and smart AI.

PEDAGOGIC ACTIVITIES

2017-2018: Teaching assistant at the Higher Institute of Applied Sciences and Technology of Sousse, University of Sousse, Sousse –Tunisia

Courses to undergraduate students;

- Design of real time systems in software engineering
- Micro programmable systems

2016-2017: Teaching assistant at the Higher Institute of Applied Sciences and Technology of Sousse, University of Sousse, Sousse –Tunisia

Courses to electrical engineer students;

- Integrated circuits: combinational and sequential logic
- VHDL Synthesis: crossbars for computing and FPGA implementation (Altera Quartus)
- Systems on SOC

2015-2016: Teaching assistant at the Faculty of Science of Monastir, Monastir – Tunisia

Courses to undergraduate students;

- Circuit design in spice simulator

2014-2015: Teaching assistant at the Faculty of Sciences of Monastir, Monastir – Tunisia

Courses to undergraduate students;

- Computer assisted design (CAO)

INDUSTRIAL EXPERIENCE

31 July – 31 August 2013: TOTAL GAS Tunisia:

- Participation to the implementation team of engineers with new management system software for maintenance, instruments and production.
- Plan and manage production activities.
- Ensure efficiency and quality in the daily production process.
- Coordinate the activities of maintenance and security of the machines

01 July - 31 July 2012: Express Elevator LG:

- Prepare documentations for the assessment of the elevator installation: Energy consumption, reliability, comfort, security, sensors...
- Make checks lists on the preventive maintenance and measurements.
- Work in the customer service “on site elevator reparation”
- Attend a training tutorial on the prevention against risks of accidents.

July - August 2012: TUNISAIR: The flag carrier airline of Tunisia

The complex technique and the department of management quality:

- Workshop of No Destructive Controls, Automatism and electronic control workshop, Workshop calibration: calibrate and verify sensors and instruments of measure.
- Engineering Service: Survey of reliability and the safety of brake working and wheel.
- HVAC (Heating, Ventilating, and Air Conditioning) department.

31 July - 31 August 2011: The Central Laboratory of Analyses and Tests: Department of Industrial Metrology.

- Prepare cards of lifetime for sensors and measuring instruments.
- Participate in the management of the equipment: protection, storage, and handling.
- Calibration and/or verification of measuring instruments on site, in company and in laboratories: Strength and couple, Temperature, Mass, Pressure and Dimensional.

PERSONAL SKILLS

Mother tongue(s): Arabic

Foreign language(s)

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken interaction	Spoken production	
French	C1	C1	C1	C1	C1
English	C1	C1	C1	C1	C1
Spanish	A2	A2	A2	A2	A1
Portuguese	A2	A2	A2	A2	A1

Italian	A1	A1	A1	A1	A1

Levels: A1 and A2: Basic user - B1 and B2: Independent user - C1 and C2: Proficient user
Common European Framework of Reference for Languages

Communication skills

- Effective communication skills

Organisational / managerial skills

- Skills gained through my experience as leader of a Scout unit:
- Leadership skills and work within a team
- Ability to work well with others in a collaborative environment
- Job skills under pressure
- Discipline
- Manage time effectively

Job-related skills

- Good working knowledge of Integrated circuit design software: Cadence, Mentor graphics, tanner, ADS…
- Good working knowledge on Deep learning algorithms for computer vision applications.
- Good knowledge of programming language (C/C++, Python, Verilog-a, Vhdl,, Matlab).
- Good knowledge of IC design and computer architectures (Spice, Virtuoso, Layout-Post layout, FPGA, Asic).
- Good working knowledge of physical modeling software: COMSOL, SILVACO, HFSS.
- Good command of Microsoft Office™ tools: Excel, Origin 8, Word, PowerPoint, Visio Project, Publisher.

Digital skills

SELF-ASSESSMENT				
Information processing	Communication	Content creation	Safety	Problem solving
Proficient user	Proficient user	Proficient user	Proficient user	Proficient user

Digital skills - Self-assessment grid

Other skills

- Photography
- Reading
- Human Development:
  - Time Management
  - Science of creativity
  - How optimistic are planted in your life
  - The power of positive thinking Secrets of success
  - Motivations

ADDITIONAL INFORMATION

Technical skills

- Electronic: Digital and Analog.
- Automatic: Continuous and discrete.
- Signal processing.
- Computers: programming
- Physics of devices
- AI on the edge